**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

**Listing of Claims:**

1-172. (Canceled)

173. (previously amended) An electronic substrate having a plurality of semiconductor devices, comprising:

a substrate;

a thin film of nanowires, deposited on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions; and

one or more pairs of source and drain contacts formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices, wherein at least two or more nanowires within said thin film of nanowires form a channel between each of said respective pairs of source and drain contacts.

174. (canceled).

175. (previously amended) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises diodes, and wherein said one or more pairs of source and drain contacts comprise anode and cathode electrodes formed above or below said thin film of nanowires.

176. (original) The semiconductor devices of claim 175, wherein said thin film of nanowires forms a p-n junction between said anode and cathode electrodes.

177. (original) The semiconductor devices of claim 175, wherein said diodes comprise light emitting diodes.

178. (original) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises logic devices.

179. (original) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises memory devices.

180. (original) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices comprises an active matrix driving circuit.

181. (original) The semiconductor devices of claim 173, wherein said nanowires are aligned substantially parallel to their long axis.

182. (previously amended) The semiconductor devices of claim 173, wherein the nanowires are aligned approximately parallel to an axis between the source and drain contacts.

183. (previously amended) The semiconductor devices of claim 173, further comprising one or more gate electrodes formed on the substrate, wherein said thin film of nanowires is formed on said one or more gate electrodes, and said one or more pairs of source and said drain contacts are formed on said thin film of nanowires.

184. (previously amended) The semiconductor devices of claim 173, wherein said one or more pairs of source and said drain contacts are formed on said substrate, said thin film of nanowires is formed on said source and said drain contacts, and further comprising one or more gate contacts formed on said thin film of nanowires.

185. (previously amended) The semiconductor devices of claim 183, wherein said one or more gate electrodes and said one or more pairs of source and drain contacts are formed on said substrate, and said thin film of nanowires is formed on said one or more gate electrodes and said one or more pairs of source and drain contacts.

186. (previously amended) The semiconductor devices of claim 183, wherein said one or more gate electrodes and said one or more pairs of source and drain contacts are formed on said thin film of nanowires.

187. (original) The semiconductor devices of claim 173, further comprising interconnects between a subset of the semiconductor devices.

188. (original) The semiconductor devices of claim 173, wherein said substrate comprises a flexible thin film.

189. (original) The semiconductor devices of claim 173, wherein said substrate comprises transparent material.

190. (original) The semiconductor devices of claim 173, wherein said substrate comprises a transparent material.

191. (original) The semiconductor devices of claim 173, wherein said nanowires are single crystal nanowires, wherein electric carriers transport through said single crystal nanowires with a mobility comparable to that of electric carriers transporting in a device formed from traditional planer single crystal semiconductor materials

192. (previously amended) The semiconductor devices of claim 173, wherein said thin film of nanowires comprises a sufficient number of nanowires to have a on state current level in the channels of greater than 10 nanoamps.

193. (previously amended) The semiconductor devices of claim 173, wherein said channels comprise more than one nanowire.

194. (previously amended) The semiconductor devices of claim 183, at least a subset of said gate electrodes comprise more than one thin film of nanowires.

195. (previously amended) The semiconductor devices of claim 173, wherein at least a subset of the channels comprises a p-n junction, whereby during operation the p-n junctions emit light.

196. (original) The semiconductor devices of claim 173, wherein said nanowires are doped.

197. (original) The semiconductor devices of claim 173, wherein at least a subset of said nanowires have doped cores.

198. (original) The semiconductor devices of claim 173, wherein at least a subset of said nanowires have doped shells.

199. (original) The semiconductor devices of claim 173, wherein at least a subset of said nanowires have doped cores and shells.

200. (previously amended) The semiconductor devices of claim 173, wherein at least a subset of said nanowires are oxidized to thereby form a gate dielectric.

201. (original) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices are electrically coupled to another circuit.

202. (original) The semiconductor devices of claim 201, wherein said circuit is a logic circuit.

203. (original) The semiconductor devices of claim 201, wherein said circuit is a memory circuit.

204. (original) The semiconductor devices of claim 201, wherein said circuit is an active matrix driver circuit.

205. (original) The semiconductor devices of claim 173, wherein at least a subset of the semiconductor devices are physically coupling to another circuit.

206. (original) The semiconductor devices of claim 205, wherein said circuit is a logic circuit.

207. (original) The semicónductor devices of claim 205, wherein said circuit is a memory circuit.

208. (original) The semiconductor devices of claim 205, wherein said circuit is an active matrix driver circuit.

209. (original) The semiconductor devices of claim 173, wherein said nanowires are patterned.

210. (original) The semiconductor devices of claim 209, wherein said patterned nanowires are photolithography patterned.

211. (original) The semiconductor devices of claim 209, wherein said patterned nanowires are screen printed.

212. (original) The semiconductor devices of claim 209, wherein said patterned nanowires are ink-jet printed.

213. (original) The semiconductor devices of claim 209, wherein said patterned nanowires are micro-contact printed.

214. (original) The semiconductor devices of claim 173, wherein the nanowires are spin casted.

215. (original) The semiconductor devices of claim 173, wherein the nanowires are mechanically aligned.

216. (original) The semiconductor devices of claim 173, wherein the nanowires are flow-aligned.

217. (original) The semiconductor devices of claim 173, wherein the nanowires are shear-force aligned.

218. (original) The semiconductor devices of claim 173, wherein said nanowires comprise sufficient density to have statistic probability of achieving a device anywhere on the substrate.

219. (original) The semiconductor devices of claim 173, further comprising a layer of oxide deposited on at least a portion of said nanowires.

220. (original) The semiconductor devices of claim 173, wherein said nanowires are ballistic conductors having a mobility greater than that of single crystal semiconductor material.

221. (original) The semiconductor devices of claim 173, wherein said nanowires are randomly oriented.

222. (original) The semiconductor devices of claim 173, wherein said nanowires are a formed as a monolayer film, a sub monolayer film, or a multi layer film.

223. (cancelled)

224. (previously amended) A method of making an electronic substrate having a plurality of semiconductor devices, comprising:

(a) depositing on a substrate a thin film of nanowires with a sufficient density of nanowires to achieve an operational current level;

(b) defining a plurality of semiconductor device regions in or on the thin film of nanowires; and

(c) forming one or more pairs of source and drain contacts at the semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices, wherein at least two or more nanowires within said thin film of nanowires form a channel between each of said respective pairs of source and drain contacts.

225. (original) The method of claim 224, further comprising aligning the nanowires substantially parallel to their long axis.

226. (canceled).

227. (previously amended) The method of claim 224, further comprising a step of forming gate electrodes.

228. (original) The method of claim 224, wherein step (c) comprises forming anode and cathode electrodes.

229. (previously amended) The method of claim 224, wherein the nanowires are aligned approximately parallel to an axis between the source and drain contacts

230. (previously amended) The method of claim 227, wherein the gate electrodes are formed on the substrate, the thin film of nanowires is formed on the gate electrodes, and the one or more pairs of source and drain contacts are formed on the thin film of nanowires.

231. (previously amended) The method of claim 227, wherein the one or more pairs of source and drain contacts are formed on the substrate, the thin film of nanowires is formed on the source and drain contacts, and the gate electrodes are formed on the thin film of nanowires.

232. (previously amended) The method of claim 227, wherein the gate electrodes and the one or more pairs of source and drain contacts are formed on the substrate, and the thin film of nanowires is formed on the gate electrodes and the one or more pairs of source and drain contacts.

233. (previously amended) The method of claim 227, wherein the gate electrodes and the one or more pairs of source and drain contacts are formed on the thin film of nanowires.

234. (currently amended) A semiconductor device comprising:

a substrate;

a plurality of nanowires deposited on the substrate, wherein each of said plurality of nanowires comprises a core and one or more shell layers disposed about said core.; and

at least a first source contact and a first drain contact formed in or on the substrate providing electrical connectivity to the plurality of nanowires, wherein the plurality of nanowires form a channel between said at least first source and drain contacts.

235. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires comprises at least two or more nanowires.

236. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires comprises at least five or more nanowires.

237. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires comprises at least ten or more nanowires.

238. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires comprises at least 100 or more nanowires.

239. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires are aligned substantially parallel to their long axis.

240. (previously presented) The semiconductor device of claim 234, further comprising at least one gate contact formed above or below said plurality of nanowires.

241. (previously presented) The semiconductor device of claim 234, wherein said substrate comprises a flexible thin film.

242. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires have a sufficient density to provide an operational current level of at least about 2 nanoamps.

243. (previously presented) The semiconductor device of claim 234, wherein the plurality of nanowires have a sufficient density to provide an operational current level of at least about 10 nanoamps.

244. (cancelled).

245. (previously presented) The semiconductor device of claim 234, wherein at least one of said one or more shell layers comprises an oxidized shell layer to thereby form a gate dielectric about said core.